What is claimed is:

1. A manufacturing method of a semiconductor device, comprising the steps of:

forming a first insulating film on a first main surface of a substrate and then forming a second insulating film on a second main surface of said substrate; and

forming a wiring layer over the first main surface of said substrate.

2. A manufacturing method of a semiconductor device, comprising the steps of:

forming a first insulating film on a first main surface of a substrate and then forming a second insulating film on a bevel portion of said substrate; and

forming a wiring layer on the first main surface of said substrate.

3. A manufacturing method of a semiconductor device comprising the steps of:

forming a first insulating film on a first main surface of a substrate and then forming a second insulating film on a second main surface and a bevel portion of said substrate; and

forming a wiring layer on the first main surface of said substrate.

4. The manufacturing method of a semiconductor device according to claim 1,

wherein said second insulating film is formed on one of the whole are and a partial area of the second main

surface of said substrate.

5. The manufacturing method of a semiconductor device according to claim 4,

wherein said second insulating film is one of a TEOS oxide film, a silicon nitride film, and a silicon oxide film formed through a plasma CVD method.

6. The manufacturing method of a semiconductor device according to claim 4,

wherein said second insulating film has a thickness of about 100 nm or more.

7. The manufacturing method of a semiconductor device according to claim 4,

wherein said first insulating film covers a gate insulating film and a gate electrode of a MISFET formed over the first main surface of said substrate.

8. The manufacturing method of a semiconductor device according to claim 2,

wherein said second insulating film is formed on one of the whole area and a partial area of the bevel portion of said substrate.

9. The manufacturing method of a semiconductor device according to claim 8,

wherein said second insulating film is one of a TEOS oxide film, a silicon nitride film, and a silicon oxide film formed through a plasma CVD method.

10. The manufacturing method of a semiconductor device according to claim 8,

wherein said second insulating film has a thickness of about 100 nm or more.

11. The manufacturing method of a semiconductor device according to claim 8,

wherein said first insulating film covers a gate insulating film and a gate electrode of a MISFET formed over the fist main surface of said substrate.

12. The manufacturing method of a semiconductor device according to claim 3,

wherein the second insulating film is formed on one of the whole areas of the second main surface and the bevel portion of said substrate; the whole area of the second main surface and a partial area of the bevel portion of said substrate; a partial area of the second main surface and the whole area of the bevel portion of said substrate; and partial areas of the second main surface and the bevel portion of said substrate.

13. The manufacturing method of a semiconductor device according to claim 12,

wherein said second insulating film is one of a TEOS oxide film, a silicon nitride film, and a silicon oxide film formed through a plasma CVD method.

14. The manufacturing method of a semiconductor device according to claim 12,

wherein said second insulating film has a thickness of about 100 nm or more.

15. The manufacturing method of a semiconductor

device according to claim 12,

wherein said first insulating film covers a gate insulating film and a first gate electrode of a MISFET formed over the first main surface of said substrate.

16. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a first insulating film on a first main surface of a substrate;

(b) a step of forming a second insulating film on a second main surface of said substrate; and

(c) a step of polishing said first insulating film through a CMP method,

wherein a wiring layer is formed over the first main surface of said substrate after said step (c).

17. The manufacturing method of a semiconductor device according to claim 16,

wherein the second insulating film formed on the second main surface of said substrate covers a bevel portion of said substrate.

18. The manufacturing method of a semiconductor device according to claim 16,

wherein said second insulating film is one of a TEOS oxide film, a silicon nitride film, and a silicon oxide film formed through a plasma CVD method.

19. The manufacturing method of a semiconductor device according to claim 16,

wherein said second insulating film has a thickness of

about 100 nm or more.

20. The manufacturing method of a semiconductor device according to claim 16,

wherein a cleaning process of said substrate is performed before said step (c).

21. The manufacturing method of a semiconductor device according to claim 20,

wherein said cleaning process is performed by one of a brushing system and an ultrasonic system.

22. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a first insulating film on a first main surface of a substrate;

(b) a step of forming a second insulating film on a second main surface of said substrate;

(c) a step of polishing the first insulating film through a CMP method and then forming a connection hole in a predetermined area of said first insulating film;

(d) a step of forming a fist metallic film over the first main surface of said substrate, and polishing said first metallic film through a CMP method, and then forming a plug in said connection hole; and

(e) a step of forming a second metallic film over the first main surface of said substrate and then etching said second metallic film to form a wiring layer.

23. The manufacturing method of a semiconductor device according to claim 22,

wherein said wiring layer uses one of tungsten and aluminum as a main conductor layer.

24. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a first insulating film on a first main surface of a substrate;

(b) a step of forming a second insulating film on a second main surface of said substrate;

(c) a step of polishing said first insulating film through a CMP method and then forming a connection hole in a predetermined area of said first insulating film; and

(d) a step of forming a metallic film over the first main surface of said substrate and then etching said metallic film to form a wiring layer.

25. The manufacturing method of a semiconductor device according to claim 24,

wherein said wiring layer uses one of tungsten and aluminum as a main conductor layer.

26. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a first insulating film on a first main surface of a substrate;

(b) a step of forming a second insulating film on a second main surface of said substrate;

(c) a step of polishing the first insulating film through a CMP method and then forming a connection hole in a predetermined area of said first insulating film;

(d) a step of forming a first metallic film over the first main surface of said substrate, and then polishing said first metallic film through a CMP method, and forming a plug in said connection hole;

(e) a step of forming a third insulating film over the first main surface of said substrate and then forming a wiring groove in a predetermined area of said third insulating film; and

(f) a step of forming a second metallic film over the first main surface of said substrate, and then polishing said second metallic film through a CMP method, and forming a wiring layer in said wiring groove.

27. The manufacturing method of a semiconductor device according to claim 26,

wherein said wiring layer uses copper as a main conductor layer.

28. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a first insulating film on a first main surface of a substrate;

(b) a step of forming a second insulating film on a second main surface of said substrate;

(c) a step of polishing said first insulating film through a CMP method and then forming a third insulating film over the first main surface of said substrate;

(d) a step of forming a wiring groove in a predetermined area of said third insulating film and

forming a connection hole in a predetermined area of said first insulating film; and

(e) a step of forming a metallic film over the first main surface of said substrate, and then polishing said metallic film through a CMP method, and forming a wiring layer integral with a connection member, in said wiring groove and said connection hole.

29. The manufacturing method of a semiconductor device according to claim 28,

wherein said wiring layer uses copper as a main conductor layer.

30. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a first insulating film on a first main surface of a substrate and then forming a connection hole in a predetermined area of said first insulating film;

(b) a step of forming a metallic film on the first main surface of the substrate;

(c) a step of forming a second insulating film on a second main surface of said substrate; and

(d) a step of polishing said metallic film through a CMP method and forming a plug in said connection hole,

wherein a wiring layer is formed over the first main surface of said substrate after said step (d).

31. The manufacturing method of a semiconductor device according to claim 30,

wherein the second insulating film formed on the second main surface of said substrate covers a bevel portion of said substrate.

32. The manufacturing method of a semiconductor device according to claim 30,

wherein said second insulating film is one of a TEOS oxide film, a silicon nitride film, and a silicon oxide film formed through a plasma CVD method.

33. The manufacturing method of a semiconductor device according to claim 30,

wherein said second insulating film has a thickness of about 100 nm or more.

34. The manufacturing method of a semiconductor device according to claim 30,

wherein said plug uses one of tungsten, aluminum, and copper as a main conductor layer.

35. The manufacturing method of a semiconductor device according to claim 30,

wherein a cleaning process of said substrate is performed before said step (d).

36. The manufacturing method of a semiconductor device according to claim 35,

wherein said cleaning process is performed by one of a brushing system and an ultrasonic system.

37. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a first insulating film on a

first main surface of a substrate and then forming a connection hole in a predetermined area of said first insulating film;

(b) a step of forming a first metallic film over the first main surface of said substrate;

(c) a step of forming a second insulating film on a second main surface of said substrate;

(d) a step of polishing the first metallic film through a CMP method and forming a plug in said connection hole; and

(e) a step of forming a second metallic film over the first main surface of said substrate and then etching said second metallic film to form a wiring layer.

38. The manufacturing method of a semiconductor device according to claim 37,

wherein said wiring layer uses one of tungsten and aluminum as a main conductor layer.

39. The manufacturing method of a semiconductor device according to claim 37,

wherein said plug uses one of tungsten, aluminum, and copper as a main conductor layer.

40. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a first insulating film on a first main surface of a substrate and then forming a connection hole in a predetermined area of said first insulating film;

(b) a step of forming a first metallic film over the first main surface of said substrate;

(c) a step of forming a second insulating film on a second main surface of said substrate;

(d) a step of polishing said first metallic film through a CMP method and forming a plug in said connection hole;

(e) a step of forming a third insulating film over the first main surface of said substrate and then forming a wiring groove in a predetermined area of said third insulating film; and

(f) a step of forming a second metallic film over the first main surface of said substrate, and then polishing said second metallic film through a CMP method, and forming a wiring layer in said wiring groove.

41. The manufacturing method of a semiconductor device according to claim 40,

wherein said wiring layer uses copper as a main conductor layer.

42. The manufacturing method of a semiconductor device according to claim 40,

wherein said plug uses one of tungsten, aluminum, and copper as a main conductor layer.

43. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a gate insulating film and a gate electrode of a MISFET over a first main surface of a

substrate;

(b) a step of forming a first insulating film on the first main surface of said substrate;

(c) a step of forming a second insulating film on a second main surface of said substrate and then performing a cleaning process of said substrate;

(d) a step of forming a sidewall spacer on a sidewall of the gate electrode of said MISFET by etching said first insulating film;

(e) a step of forming a source and drain of said MISFET;

(f) a step of forming a third insulating film over the first main surface of said substrate and then forming a connection hole in a predetermined area of said third insulating film; and

(g) a step of forming a wiring layer over the first main surface of said substrate.

44. The manufacturing method of a semiconductor device according to claim 43,

wherein the cleaning process applied to said substrate in said step (c) is performed by one of a brushing system and an ultrasonic system.

45. A manufacturing method of a semiconductor device, comprising:

(a) a step of forming a gate insulating film of a MISFET on a first main surface of a substrate;

(b) a step of forming a conductive film on the first

main surface of said substrate;

(c) a step of forming a first insulating film on a second main surface of said substrate and then performing a cleaning process of said substrate;

(d) a step of forming a gate electrode of said MISFET by etching said conductive film;

(e) a step of forming a second insulating film over the first main surface of said substrate and then forming a sidewall spacer on a sidewall of the gate electrode of said MISFET by etching said second insulating film;

(f) a step of forming a source and drain of said MISFET;

(g) a step of forming a third insulating film over the first main surface of said substrate and then forming a connection hole in a predetermined area of said third insulating film; and

(h) a step of forming a wiring layer over the first main surface of said substrate.

46. The manufacturing method of a semiconductor device according to claim 45,

wherein the cleaning process applied to said substrate in said step (c) is performed by one of a brushing system and an ultrasonic system.